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Abstract. Parallel algorithms are normally designed for execution on networks of N processors, with N depending on the size of the problem to be solved. In order that a parallel algorithm can be executed on a concrete, fixed size network in practice, one can attempt to map (simulate) the unrestricted network on the smaller network. For networks that use direct connections (links) between pairs of processors, a suitable notion of simulation, termed emulation, was introduced by Fishburn and Finkel [7]. We extend the concept to the realistic case of networks that use buses, i.e. connections between arbitrary large sets of processors, as well. Several emulations of the spanning bus hypercube and the dual bus hypercube on smaller networks of the same type are given.

1. <u>Introduction</u>. Parallel algorithms are normally designed for execution on networks of N processors, with N depending on the size of the problem to be solved. In practice there will be a varying problem size, but a fixed network size. The resulting disparity between algorithm design and implementation must be resolved by simulating a network of some size N on a fixed and smaller size network of a similar or different kind, in a structure preserving manner. For networks that use links, i.e. connections between pairs of processors a notion of simulation, termed emulation was proposed by Fishburn and Finkel [7].

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Independently Berman [1] proposed a similar notion. The interconnection structure of this kind of networks is generally represented by a (possibly directed) graph.

<u>Definition</u>. Let $G=(V_G, E_G)$ and $H=(V_H, E_H)$ be networks of processors (graphs). We say that G can be emulated on H if there exists a function $f: V_G \to V_H$ such that for every edge $(v, v') \in E_G: f(v)=f(v')$ or $(f(v), f(v')) \in E_H$. The function f is called an emulation function or, in short, an emulation of G on H.

Let f be an emulation of G on H. Any processor w $\in V_H$ must actively emulate the processors $e f^{-1}(w)$ in G. When $v \in f^{-1}(w)$ communicates information to a neighbouring processor v', then h must communicate the corresponding information "internally", when it emulates v' itself, or to a neighbouring processor w'=f(v') in H otherwise. If all processors act synchronously in G, then the emulation will be slowed by a factor proportional to max $|f^{-1}(w)|$.

<u>Definition</u>. Let G, H and f be as above. The emulation f is said to be (computationally) uniform if for all w,w' $\in V_H$: $|f^{-1}(w)| = |f^{-1}(w')|$.

Every uniform emulation f has associated with it a fixed constant c, called: the computation factor, such that for all $w \in V_H |f^{-1}(w)| = c$. It means that every processor of H emulates the same number of processors of G.

In [7] it was observed, that an emulation f of $G=(V_G, E_G)$ on $H=(V_H, E_H)$ induces a mapping $f': E_G \rightarrow V_H \cup E_H$ in a natural way: $f'((v_1, v_2)) = f(v_1)$ iff $f(v_1) = f(v_2)$ and $f'((v_1, v_2)) = (f(v_1), f(v_2))$ iff $(f(v_1), f(v_2)) \in E_H$.

An extensive analysis of (uniform) emulations was made by Bodlaender and van Leeuwen [3-6].

The given concept of emulation can be used for networks that use links for communication (only). However, a realistic processor network

can also use buses for communication. Theoretically, a bus connects an arbitrary set of processors. An advantage of the use of buses is that one can keep the diameter of the network (the maximum number of hops needed to go from one processor to another processor) low, without having a large number of connections per processor. In [9] one can find a comparison between a number of different interconnection schemes, including three networks with buses: the "global bus" (all processors are connected to one bus), the "spanning bus hypercube" and the "dual bus hypercube" (for definitions see section 4). In this paper we extend the notion of emulation to networks that use buses for communication. In section 2 we show how to model the interconnection structure of a network with buses by means of hypergraphs. Hypergraphs appear to be a natural way to model networks with buses and allow a formal reasoning about these networks without much difficulty. In section 3 we extend the notion of emulation to hypergraphs, and define the computation and communication cost of emulations. In section 4 we give efficient emulations of the spanning bus hypercube and the dual bus hypercube, which are the most common architectures of bus-networks (cf. Wittie [9]). Some final remarks are made in section 5.

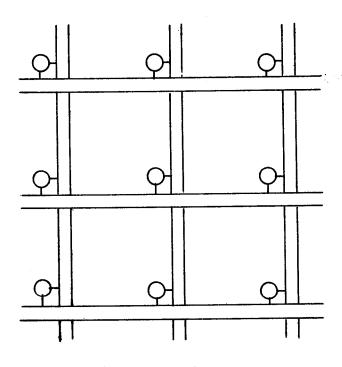
2. The hypergraph model. The interconnection structure of a network that uses links for communication is usually represented by a (possibly directed) graph. For representing the interconnection structure of networks with buses the graph model seems to be inadequate. Each processor connected to a bus can send messages via the bus, to some subset of the processors that are connected to the bus. There cannot be more than one message simultaneously on the same bus. Therefore it does not seem appropriate to replace all the processors connected to the same bus by a clique, (which would result in a graph with edges between nodes v_1, v_2 iff there is a bus to which v_1 and v_2 are connected). In this way one loses (possibly) essential information about the interconnection structure of the network. For instance the global bus network ("all processors are connected to a single bus") is replaced by a complete graph. However a network with a link between each pair of processors allows much more simultaneous message traffic

than a global bus network does.

A natural model for networks with buses is provided by <u>hypergraphs</u>. A hypergraph is a 2-tuple (V,E), with V a set of nodes, and E a collection of subsets of V (edges), with

- (i) e e E ⇒e ≠ Ø
- (ii) $\frac{U}{eEE} = V$.

For the theory of hypergraphs, see e.g. [2]. The processors of the network correspond to the nodes of the hypergraph, the (links and) buses to the edges. We denote edges by a,b,c,d,e, and nodes by v,w,x,y,z. If processor v is connected to bus b, then v e b, in the hypergraph. Note that the hypergraph is not necessarily simple: multiple busses can connect the same set of nodes. For an example of a network with buses and its hypergraph, see fig. 2.1. and fig. 2.2.



0 = processor

-- = bus

fig. 2.1.

A processor network with 9 processors and 6 buses

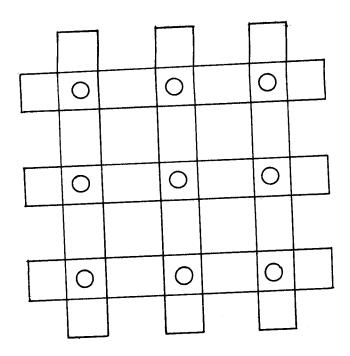


fig. 2.2. The corresponding hypergraph with 9 nodes and 6 edges

It is possible that processor networks use a combination of links and buses. Links can be full-duplex (the two processors can send a message to each other simultaneously), halfduplex (at most one processor can send at a time) or simplex (messages can be send only in one direction). Half-duplex links can be treated as buses with two connected processors. To incorporate the other two types of links in our model, we define "directed hypergraphs". A directed hypergraph is a 2-tuple (V,E), with V a set of nodes and E a collection of ordered pairs of subsets of V (edges), with

- (i) (d,e) $\in E \Rightarrow (d \neq \emptyset \land e \neq \emptyset)$
- (ii) $U \{e \mid \exists d (d,e) \in E\} = V$
- (iii) $U \{d | \exists e (d,e) \in E\} = V.$

Each node in V represents a processor, each edge (d,e) in E a communication medium. The nodes in d represent processors that can send messages via the medium; the nodes in e represent processors that can receive messages via the medium. For a bus (d,e) one has d=e. Full-

duplex links are replaced by two simplex links.

3. Emulations of hypergraphs. Unlike in the case of graph emulations, a mapping of the nodes V_G of a hypergraph $G=(V_G,E_G)$ on the nodes V_H of a hypergraph $H=(V_H,E_H)$ does not immediately induce a mapping of E_G on V_H U E_H . Therefore we include the mapping of E_G on V_H U E_H explicitly in the definition of an emulation.

<u>Definition</u>. Let $G=(V_G, E_G)$, $H=(V_H, E_H)$ be hypergraphs. A mapping $f: V_G \cup E_G \rightarrow V_H \cup E_H$ is an <u>emulation</u> function (in short: an <u>emulation</u>) of G on H, if and only if

- (i) $f(V_G) \subseteq V_H$, and
- (ii) For all $v \in V_G$, $e \in E_G$, $v \in e$: $f(e) \in V_H \Rightarrow f(v) = f(e)$ and $f(e) \in E_H \Rightarrow f(v) \in f(e)$.

Clearly, emulation is transitive. (If f emulates G on H, and g emulates H on K, then g o f emulates G on K.) For (undirected) graphs (seen as hypergraphs with each edge cardinality 2) the new definition of emulation coincides with the old definition. Let f be an emulation of graph $G=(V_G,E_G)$ on graph $H=(V_H,E_H)$ (by the new definition), and suppose $(v_1,v_2) \in E_G$. If $f((v_1,v_2)) \in V_H$, then $f(v_1) \in f((v_1,v_2))$ and $f(v_2) \in f((v_1,v_2))$, so $f(v_1)=f(v_2)$ or $(f(v_1),f(v_2)) \in E_H$.

Let f be an emulation of hypergraph $G=(V_G,E_G)$ on hypergraph $H=(V_H,E_H)$. Any processor we V_H must actively emulate the processors in $f^{-1}(w) \cap V_G$. When $v \in f^{-1}(w) \cap V_G$ communicates information via a bus b to neighbouring processors $x_1,\ldots,x_m \in b$, them w must either communicate the corresponding information internally (iff $w=f(b) \in V_H$), or communicate the information via bus f(b) to the processors $f(x_1),\ldots,f(x_m)$, (iff $f(b) \in E_H$).

To determine the factor by which the emulation "slows down" a computation on the network we distinguish between the time needed for computations inside the processors, and the time needed for communication between the processors. If all processors act synchronously in G, then the time needed for computations will be increased by a factor, proportional to max $|f^{-1}(w) \cap V_G^-|$.

Definition. Let f emulate hypergraph $G=(V_G,E_G)$ on hypergraph $H=(V_H,E_H)$. The computation cost of f is $cc(f)=\max_{w\in V_H}|f^{-1}(w)\cap V_G|$.

<u>Definition</u>. Let f be as above. f is computationally uniform, iff $cc(f) = |V_G|/|V_H|$.

It means that for a computationally uniform emulation f, for every processor w $\in V_H$, $|f^{-1}(w) \cap V_G| = cc(f)$: every processor w in H emulates the same number of processors in G.

The factor by which the communication time is slowed down can be estimated by max $|f^{-1}(e)|$ (=the maximum number of buses a bus has to e^{eE}_H

emulate.) This factor can be 0, in the degenerate case that all processors that can communicate with each other are mapped on the same node. In general all processors can communicate with each other using one or more communication steps (i.e. the hypergraph is "connected"), so if for an emulation f of a connected network G on a network H the maximum is 0, then f maps every node of G on the same node of H. In general, there will be at least one eee_H , with $f^{-1}(e) \neq d$. The factor eee_H

bus e=f(b) once every max $|f^{-1}(e)|$ timesteps. (The estimation is not $e^{eE}H$

necessarily optimal, but in general it is.)

Definition. Let f emulate hypergraph $G=(V_G,E_G)$ on hypergraph $H=(V_H,E_H)$. The communication cost of f is $comc(f) = max |f^{-1}(e)|$.

<u>Definition</u>. Let f be as above. f is communicationally uniform, iff for all $e \in E_H$ $|f^{-1}(e)| = comc(f)$.

Again, computationally uniform, and communicationally uniform emulations are transitive as relations. For directed hypergraphs, the definition of emulation becomes as follows:

<u>Definition</u>. Let $G=(V_G, E_G)$ and $H=(V_H, E_H)$ be directed hypergraphs. $f:V_G \cup E_G \rightarrow V_H \cup E_H$ is an emulation function (in short: an emulation) of G on H, iff

- (i) $f(V_G) \subseteq V_H$
- (ii) For all $v,w \in V_H = (a,b) \in E_G$, $v \in a$, $w \in b$: $f(e) \in V_H \Rightarrow f(v) = f(w) = f(e)$ and $f(e) \in E_H \Rightarrow$ one can write f(e) = (c,d), with $f(a) \in c$, $f(b) \in d$.

The definitions of computation and communication cost, and of computationally and communicationally uniform are the same for hypergraphs and directed hypergraphs.

For graphs (seen as hypergraphs with each edge of cardinality 2) and directed graphs (seen as directed hypergraphs, with each edge consisting of an ordered pair of sets, each with one element) the definitions of "computationally uniform" coincide with the old definition of "(computationally) uniform" [3,7].

4. Emulations of common networks with buses.

4.1. Emulations of the spanning bus hypercube. The d-dimensional spanning bus hypercube with width n has nodes, that can be seen as if they lie in a nxnx...xn integer grid with dimension d. That is, each node can be specified with d integer coordinates in the range {0,...,n-1}. Each node is connected to d buses, each bus going in a different dimension, connecting all the nodes whose coordinates agree in all other dimensions.

Definition. The d-dimensional spanning bus hypercube with width n is

the hypergraph
$$SB^{d,n} = (V^{d,n}, E^{d,n})$$
, with $V^{d,n} = \{(x_1, x_2, \dots, x_d) \mid \forall i, 1 \leq i \leq d : 0 \leq x_i \leq n-1\}$ and $E^{d,n} = \{e_{x_1, \dots, x_{i-1}} x_{i+1}, \dots, x_d, i \mid x_1, \dots, x_{i-1}, x_{i+1}, \dots, x_d \in \{0, \dots, n-1\}, 1 \leq i \leq d\}$, with $e_{x_1, \dots, x_{i-1}} x_{i+1}, \dots, x_d, i = \{(x_1, \dots, x_{i-1}, x_i, x_{i+1}, \dots, x_d) \mid 0 \leq x_i \leq n\}$.

An example with d=3, and n=4 is given in fig. 4.1.

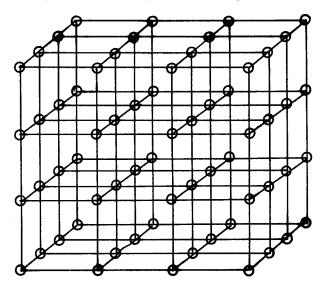


fig. 4.1.

3-dimensional spanning bus hypercube with width 4.

The one-dimensional spanning bus hypercubes are the global bus networks. The spanning bus hypercubes with width 2 are very similar to the cube networks. For an analysis of the emulations of the cube networks see [3].

One can emulate the d-dimensional spanning bus hypercube on the d-k-dimensional spanning bus hypercube with the same width for any $1 \le k \le d-1$ by a straightforward projection.

Theorem 4.1.1. The function
$$f: V^{d,n} \cup E^{d,n} \to V^{d-k,n} \cup E^{d-k,n}$$
, given by $-f((x_1, \ldots, x_d)) = (x_1, \ldots, x_{d-k})$ and $-f(e_{x_1, \ldots, x_{i-1} x_{i+1}, \ldots, x_d, i}) = e_{x_1, \ldots, x_{d-k}, i}$ iff $i \le d-k$ and $-f(e_{x_1, \ldots, x_{i-1} x_{i+1}, \ldots, x_d, i}) = (x_1, \ldots, x_{d-k})$ iff $i > d-k$

is a computationally and communicationally uniform emulation of $SB^{d,n}$ on $SB^{d-k,n}$ (d,k,d-k,ne N⁺), with $ce(f)=comc(f)=n^k$.

Proof.

It is clear that $f(V^{d,n}) \subseteq V^{d-k,n}$. Consider node $x=(x_1,\ldots,x_d) \in V^{d,n}$ and edge $e=e_{x_1,\ldots,x_{d-k},i} \in E^{d-k,n}$. If $i \le d-k$ then $f(e) \in E^{d-k,n}$, and $f(x)=(x_1,\ldots,x_{d-k}) \in e_{x_1,\ldots,x_{d-k},i} \in e_{x_1,\ldots,x_{d-k},i} = f(e)$. If i > d-k, then $f(e) \in V^{d-k,n}$ and $f(x)=(x_1,\ldots,x_{d-k})=f(e)$. So f is an emulation.

For all y (y_1, \dots, y_{d-k}) \in $V^{d-k, n}$, $|f^{-1}(y) \cap V^{d, n}| = |\{(y_1, \dots, y_{d-k}, y_{d-k+1}, \dots, y_d) \mid y_{d-k+1}, \dots, y_d \in \{0, \dots, n-1\}\}| = n^k$. So f is computationally uniform with $cc(f) = n^k$. For all $e = e_{y_1 \dots y_{i-1} y_{i+1} \dots y_{d-k}, i} \in E^{d-k, n}$, $|f^{-1}(e)| = |\{e_{y_1 \dots y_{i-1} y_{i+1} \dots y_d, i} \mid y_{d-k+1}, \dots, y_d \in \{0, \dots, n-1\}\}| = n^k$. So f is communicationally uniform with $comc(f) = n^k$. \square

For the next result, let c be any integer with c | n.

Theorem 4.1.2. The function
$$f:V^{d,n} \cup E^{d,n} \rightarrow V^{d,\frac{n}{c}} \cup E^{d,\frac{n}{c}}$$
, given by $-f((x_1,\ldots,x_d)) = (x_1 \bmod \frac{n}{c},x_2 \bmod \frac{n}{c},\ldots,x_d \bmod \frac{n}{c})$ and $-f(e_{x_1,\ldots,x_d,i}) = (x_1 \bmod \frac{n}{c},\ldots,x_d,i)$

 $(x_1 \bmod \frac{n}{c}) \dots (x_{i-1} \bmod \frac{n}{c}) (x_{i+1} \bmod \frac{n}{c}) \dots (x_d \bmod \frac{n}{c}), i$ is a computationally and communicationally uniform emulation of SB^d, n on SB^d, n/c (d,n,c \in N⁺, c|n), with cc(f)=c^d; comc(f)=c^{d-1}.

Proof.

It is clear that $f(V^{d,n}) \subseteq V$ Consider $x = (x_1, \dots, x_d) \in V^{d,n}$ and $e = e_{x_1 \dots x_{i-1} x_{i+1} \dots x_d, i}$ $e \in E^{d,n}$. f(e)eE and $f(x) = (x_1 \bmod \frac{n}{c}, \dots, x_d \bmod \frac{n}{c})$ $e \in (x_1 \bmod \frac{n}$

For all $y = (y_1, \dots, y_d) \in V^{d,n/c}$, $|f^{-1}(y) \cap V^{d,n}| = |\{(x_1, \dots, x_d) | \forall_i, 1 \le i \le d \mid x_i \mod \frac{n}{c} = y_i\}| = c^d$. So f is computationally uniform with $cc(f) = c^d$.

For all $e = e_{y_1 \dots y_{i-1} y_{i+1} \dots y_d, i}$, $|f^{-1}(e)| = |\{e_{x_1 \dots x_{i-1} x_{i+1} \dots x_d, i} | \forall j, 1 \le j \le d, j \ne i; x_j \mod e = y_j\}| = e^{d-1}$. So f is communicationally uniform with $comc(f) = e^{d-1}$. \square

4.2. Emulations of the dual bus hypercube. Wittie [9] proposed a variant of the spanning bus hypercube, which uses significantly fewer connections per node: the dual bus hypercube. Nodes in the dual bus hypercube can again be seen as points in a d-dimensional integer grid of size nxnx...xn, with n+1≥d≥2. In the dual bus hypercube each node is connected to two buses. In one dimension, say the first, buses connect nodes, as in the spanning bus hypercube. (These are n^{d-1} buses. each connected to n nodes.) Look at the d-1 dimensional layers, that are perpendicular on these buses. In the first layer, buses go in the second dimension, each connecting n nodes that agree in all but the second coordinate. In the second layer, buses go in the third dimension, etc., so in the j'th layer, buses go in the $2+(j-1) \mod (d-1)$ 'th dimension. In each layer there are n^{d-2} buses, each connected to n nodes. The advantage of a dual-bus hypercube over the spanning bus hypercube is that each node has only two connections to a bus. The diameter of the network however is 2d-1, only a factor of about 2 larger than the diameter of the spanning bus hypercube (=d).

Definition. The d-dimensional dual bus hypercube with width n is the hypergraph DB^d, n = $(V^{d}, n, \tilde{E}^{d}, n)$, with $V^{d}, n = \{(x_1, ..., x_d) | \forall i, 1 \le i \le d: 0 \le x_i \le n-1\}$ and $\tilde{E}^{d}, n = \{e_{x_1, ..., x_{i-1}, x_{i+1}, ..., x_d, i} | x_1, ..., x_{i-1}, x_{i+1}, ..., x_d \in \{0, ..., n-1\}$ and $(i=1 \text{ or } (2 \le i \le d \land i = 2 + (x_1 - 1) \mod (d-1)))\}$, with $e_{x_1, ..., x_{i-1}, x_{i+1}, ..., x_d, i} = \{(x_1, ..., x_{i-1}, x_i, x_{i+1}, ..., x_d) | 0 \le x_i \le n-1\}$.

For d=1 and d=2 the d-dimensional dual bus hypercube $DB^{d,n}$ and the d-dimensional spanning bus hypercube are the same. One has to take $n+1 \ge d$, to let the dual bus hypercube be connected.

An example of the dual bus hypercube, with d=3 and w=4 is given in fig. 4.2.

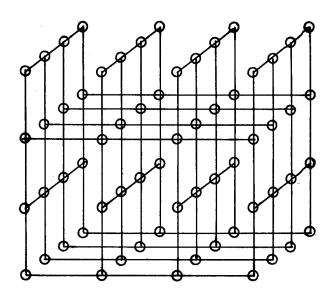


fig.4.2.
3 dimensional dual bus hypercube with width 4.

For the projections of the dual bus hypercubes on lower dimensional dual bus hypercubes with the same width we need the following result:

Lemma 4.2.1. Let d,d',n $\in \mathbb{N}^+$, and d>d' \geq 2. There is a bijection ψ^d ,d',n from $\{0,\ldots,n-1\}$ to $\{0,\ldots,n-1\}$, such that if $(x-1) \mod (d-1)+2 \leq d'$ then $(x-1) \mod (d-1)+2 = (\psi^d,d',n(x)-1) \mod (d'-1)+2$.

Proof.

For each i in $\{2,\ldots,d'\}$, one has that $|\{x\mid 0\leq x\leq n-1 \text{ and } (x-1)\mod(d-1)+2=i\}| \leq |\{x\mid 0\leq x\leq n-1 \text{ and } (x-1)\mod(d'-1)+2=i\}|$. So we can map all x with $(x-1)\mod(d-1)+2\leq d'$ in a one-to-one manner, such that $(x-1)\mod(d-1)+2=(\psi^{d},d',n(x)-1)\mod(d'-1)+2$, and map the x with $(x-1)\mod(d'-1)+2>d'$ onto the remaining nodes. \square

Theorem 4.2.2. Let d,d',n and $\psi=\psi^{d,d',n}$ be as above. The function $f:V^{d,n}$ U $\widetilde{\mathbb{E}}^{d,w} \to V^{d',n}$ U $\widetilde{\mathbb{E}}^{d',n}$, given by

-
$$f((x_1,...,x_d)) = (\psi(x_1),x_2,...,x_d)$$
 and

-
$$f(e_{x_1...x_{i-1}x_{i+1}...x_d,i}) = e_{x_2...x_d,i}$$
, iff i=1 and

$$-f(e_{x_1...x_{i-1}x_{i+1}...x_d,i}) = e_{\psi(x_1)x_2...x_{i-1}x_{i+1}...x_d,i}, \text{ iff } 2 \le i \le d'$$
and

-
$$f(e_{x_1...x_{i-1}x_{i+1}...x_d,i}) = (\psi(x_1),x_2,...,x_d), iff i>d',$$

is a computationally and communicationally uniform emulation of $DB^{d,n}$ on $DB^{d',n}$, with $cc(f) = comc(f) = n^{d-d'}$.

Proof.

First we have to show that f is a correct mapping, i.e. we have to show that for $2 \le i \le d'$, if $e_{x_1 \cdots x_{i-1} x_{i+1} \cdots x_d, i}$ $e_{\psi(x_1) x_2 \cdots x_{i-1} x_{i+1} \cdots x_d, i}$ $e_{\widetilde{E}^{d,n}}$. This is because $e_{x_1 \cdots x_{i-1} x_{i+1} \cdots x_d, i}$ $e_{\widetilde{E}^{d,n}} \Rightarrow i = 2 + (x_1 - 1) \mod (d-1) \Rightarrow (\text{use that } i \le d')$ $2 + (x_1 - 1) \mod (d-1) = 2 + (\psi(x_1) - 1) \mod (d'-1) = i \Rightarrow e_{\psi(x_1) x_2 \cdots x_{i-1} x_{i+1} \cdots x_d, i}$ $e_{\widetilde{E}^{d',n}}$.

Now we show f is an emulation. It is obvious that $f(V^{d,n}) \subseteq V^{d',n}$. Consider $x=(x_1,\ldots,x_d)\in V^{d,n}$ and edge $e=e_{x_1\ldots x_{i-1}x_{i+1}\ldots x_d}$, if i=1, then $f(x)=(\psi(x_1),x_2,\ldots,x_d)\in e_{x_2\ldots x_d}$, if i=f(e). If $2\le i\le d'$, then $f(x)=(\psi(x_1),x_2,\ldots,x_d)\in e_{\psi(x_1)x_2\ldots x_{i-1}x_{i+1}\ldots x_d}$, if i>d, then $f(x)=(\psi(x_1),x_2,\ldots,x_d)\in e_{\psi(x_1)x_2\ldots x_{i-1}x_{i+1}\ldots x_d}$, if i>d, then $f(x)=(\psi(x_1),x_2,\ldots,x_d)\in e_{\psi(x_1)}$. Hence f is an emulation.

For all $y=(y_1, \dots, y_d) \in V^{d',n}$, $|f^{-1}(x) \cap V^{d,n}| = |\{(\psi^{-1}(y_1), y_2, \dots, y_d, y_{d'+1}, \dots, y_d) \mid y_{d'+1}, \dots, y_d \in \{0, \dots, n-1\}\}| = n^{d-d'}$. (We use that ψ is bijective.) Hence f is computationally uniform and $cc(f) = n^{d-d'}$.

For all $e=e_{y_2...y_{d},1}$, $|f^{-1}(e)| = |\{e_{y_2...y_{d},1}|y_{d'+1},...,y_{d} \in \{0,...,n-1\}\}| = n^{d-d'}$. For all $e=e_{y_1...y_{i-1}y_{i+1}...y_{d}}$, i, with $2 \le i \le d'$, $|f^{-1}(e)| = |\{e_{\psi^{-1}(y_1)y_2...y_{i-1}y_{i+1}...y_{d},y_{d'+1}...y_{d},i}, |y_{d'+1},...,y_{d} \in \{0,...,n-1\}\}| = n^{d-d'}$. Hence f is communicationally uniform, and

 $comc(f) = n^{d-d'}$.

Theorem 4.2.3. Let d,n,c $\in \mathbb{N}^+$, $c \mid n$, $(d-1) \mid (\frac{n}{c})$.

The function $f: V^{d,n} \cup \widetilde{E}^{d,n} \to V$ $\int_{0}^{d,n} U^{d,n} \cup U^{d,n} \cup U$ $\int_{0}^{d,n} U^{d,n} \cup U^{d,n} \cup U$ $\int_{0}^{d,n} U^{d,n} \cup U$ $\int_{0}^{d,n} U^{d,n} \cup U$ $\int_{0}^{d,n} U^{d,n} \cup U$ $\int_{0}^{d,n} U^{d,n} \cup U$ $\int_{0}^{d,n}$

 $(x_1 \mod \frac{n}{c})\dots(x_{i-1} \mod \frac{n}{c})(x_{i+1} \mod \frac{n}{c})\dots(x_d \mod \frac{n}{c}), i$ is a computationally and communicationally uniform emulation of DB^d,n on DB $(x_1 \mod \frac{n}{c})\dots(x_{i-1} \mod \frac{n}{c})\dots(x_d \mod \frac{n}{c}), i$ on DB $(x_1 \mod \frac{n}{c})\dots(x_{i-1} \mod \frac{n}{c})\dots(x_d \mod \frac{n}{c}), i$

Proof.

It is obvious that $f(V^{d,n}) \subseteq V$ of is correct mapping: $e = e \\ x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i$ $e \in e^{x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i}$ if $e^{x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i}$ (use that $e^{x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i}$) is $e^{x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i}$ (use that $e^{x_1 \cdots x_{d-1} x_{d-1} \cdots x_{d}, i}$) is $e^{x_1 \cdots x_{i-1} x_{i+1} \cdots x_{d}, i}$ (use that $e^{x_1 \cdots x_{d-1} x_{d-1} \cdots x_{d-1}, i}$) is $e^{x_1 \cdots x_{d-1} x_{d-1} \cdots x_{d-1}, i}$ (use that $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$) is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ (use that $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$) is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ is $e^{x_1 \cdots x_{d-1} x_{d-1}, i}$ if $e^$

We next consider emulations of DB^d,ⁿ on DB^d,^{n/c}, with (d-1) $\nmid \frac{n}{c}$. The next result shows that there exist efficient, non-uniform emulations of DB^d,ⁿ on DB^d,^{n/c}, if (d-1) $\nmid \frac{n}{c}$: we have an extra factor of at most 2 in the formulas for the computation and communication cost, compared with the costs of the uniform emulations of DB^d,ⁿ on DB^d,^{n/c}, with (d-1) $|\frac{n}{c}|$.

Lemma 4.2.4. Let $d,n,n' \in \mathbb{N}^+$, $n' \mid n, n' \geq d-1$. Let c=n/n'. There exists a mapping $\psi \colon \{0,\ldots,n-1\} \to \{0,\ldots,n'-1\}$, such that

- (i) $\forall x$, $0 \le x \le n-1$: $x \mod (d-1) = \psi(x) \mod (d-1)$
- (ii) $\forall y$, $0 \le y \le n'-1$: $|\psi^{-1}(y)| \le \lceil n/((d-1), \lfloor \frac{n}{d-1} \rfloor) \rceil \le 2c$.

Proof.

Write n' = k(d-1) + 1, with $0 \le l < d-1$. The mapping ψ : $\{0, \ldots, n-1\} \rightarrow \{0, \ldots, n'-1\}$, given by $\psi(x) = x \mod(k(d-1))$ fulfils property (i) and (ii): $\forall x, 0 \le x \le n-1$: $x \mod(d-1) = (x \mod(k(d-1))) \mod(d-1)$; and $\forall y, 0 \le y \le n'-1$, $|\psi^{-1}(y)| = 0$, if $y \ge k(d-1)$, and $|\psi^{-1}(y)| = |\{x \mid 0 \le x \le n-1, x \mod(k(d-1)) = y\}| = \lceil n/(k(d-1)) \rceil$, if y < k(d-1). Note that $k = \lfloor \frac{n'}{d-1} \rfloor$, and $\lceil n/(k(d-1)) \rceil = \lceil (ck(d-1) + cl)/(k(d-1)) \rceil \le 2c$.

Theorem 4.2.5. Let d,n,n', ψ ,c be as above. The function f: $V^{d,n} \cup \widetilde{E}^{d,n} + V^{d,n} \cup \widetilde{E}^{d,n'}$, given by

-
$$f((x_1,...,x_d))=(\psi(x_1),x_2 \mod n',x_3 \mod n',...,x_d \mod n')$$
 and

-
$$f(e_{x_1...x_{i-1}x_{i+1}...x_d,i}) = e_{x_2 \mod n'...x_d \mod n',i}$$
, iff i=1, and

$$f(e_{x_1...x_{i-1}x_{i+1}...x_d,i}) =$$

Proof.

We first show that f is a correct mapping. For e=e $x_2 \cdots x_d$, 1, it is clear that f(e) $\in \widetilde{E}^{d,n}$. Now let $2 \le i \le d$. e = e $x_1 \cdots x_{i-1} x_{i+1} \cdots x_d$, if $i = (x_1 - 1) \mod (d - 1) + 2$ $\Rightarrow i = (y(x_1) - 1) \mod (d -$

Finally observe that for all $y=(y_1,\ldots,y_d)\in V^{d,n'}:|f^{-1}(y)|=|\psi^{-1}(y_1)|\cdot e^{d-1}$, and for all $e=e_{x_1\cdots x_{i-1}x_{i+1}\cdots x_{d},i}=e^{\widetilde{E}^{d,n'}}:|f^{-1}(e)|=e^{d-1}$, if i=1 and $|f^{-1}(e)|=|\psi^{-1}(y_1)|\cdot e^{d-2}$, if $2\le i\le d$. The estimations of cc(f) and comc(f) now follow from lemma 4.2.4. \square

5. <u>Final remarks</u>. The problem to decide whether there exist computationally uniform emulations from a given hypergraph G on a given hypergraph H is, in general, NP-complete. For instance, this problem

contains the UNIFORM EMLATION problem for graphs as a special case. (The UNIFORM EMULATION problem asks whether a given graph G can be (computationally) uniformly emulated on a given graph H.) UNIFORM EMULATION and many subcases of it are proven to be NP-complete in [4,5,6]. One also has that the problem whether a given hypergraph can be emulated with computation cost 1 on a 2 dimensional spanning bus hypercube, with given width N in one, and M in the other dimension is NP-complete: it contains as a special case the EDGE EMBEDDING ON A GRID problem. (This problem is: given a graph G=(V,E), positive integers M,N, is there an injective function $f: V+\{1,2,\ldots,M\}$ x $\{1,2,\ldots,N\}$, such that if (u,v) \in E then $f(u)=(x_1,x_2)$, $f(v)=(y_1,y_2)$ implies $x_1=x_2$ or $y_1=y_2$, i.e. f(u) and f(v) are on the same 'line' in the grid?) EDGE EMBEDDING ON A GRID is NP-complete (see e.g. [8,p.219]).

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